

1      **CLAIMS:**

2      1. A method of forming a co-axial line comprising:  
3                providing a substrate having an outer surface;  
4                forming a conductive line at least a portion of which is  
5                elevationally spaced from the outer surface;  
6                forming a dielectric polymer layer over and surrounding at least  
7                a portion of the conductive line where it is spaced from the outer  
8                surface; and  
9                forming an outer conductive sheath over the dielectric polymer  
10              layer.

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12      2. The method of claim 1, wherein the forming of the outer  
13              conductive sheath comprises chemical vapor depositing a metal-comprising  
14              layer of material over the dielectric polymer layer.

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16      3. The method of claim 2, wherein the metal-comprising layer  
17              includes aluminum.

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19      4. The method of claim 1, wherein the dielectric polymer layer  
20              comprises Parylene.

1       5. The method of claim 1, wherein the forming of the  
2 conductive line comprises:

3              forming a conductive line pattern over the substrate outer surface;  
4              forming conductive material over and within the conductive line  
5 pattern; and

6              removing material of the conductive line pattern from elevationally  
7 below the conductive material.

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9       6. The method of claim 5, wherein the forming of the  
10 conductive material comprises:

11              forming a conductive film layer over the conductive line pattern;  
12 and  
13              electroplating conductive material over the conductive film layer.

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15       7. The method of claim 5, wherein the forming of the  
16 conductive material comprises electroless plating a conductive material  
17 over the conductive line pattern.

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19       8. A method of forming a conductive line comprising:  
20              forming conductive material within a line pattern within a layer  
21 of photoresist and over a substrate outer surface; and  
22              removing the layer of photoresist and suspending at least a portion  
23 of the conductive material in the line pattern above the substrate outer surface.

1           9. The method of claim 8, wherein the forming of the  
2 conductive material comprises electroplating a conductive material over  
3 the layer of photoresist.

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5           10. The method of claim 8, wherein the forming of the  
6 conductive material comprises electroless plating a conductive material  
7 over the layer of photoresist.

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9           11. The method of claim 8, wherein the suspending of the  
10 conductive material comprises prior to the forming of the conductive  
11 material, forming at least one terminal member over the substrate outer  
12 surface, the conductive material being formed over and support by the  
13 terminal member.

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15          12. A method of forming a co-axial line comprising:  
16              forming a masking material layer over a substrate;  
17              patterning the masking material layer to form at least one  
18              conductive line pattern;  
19              forming an inner conductive layer within the at least one  
20              conductive line pattern;  
21              vapor depositing a layer comprising a polymer dielectric material  
22              over at least some of the inner conductive layer; and  
23              forming an outer conductive layer over the polymer dielectric  
24              material.

1           13. The method of claim 12, wherein the forming of the inner  
2           conductive layer comprises:

3                 sputtering a conductive film layer over the conductive line pattern;  
4                 and

5                 electroplating a conductive material over the conductive film layer.

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7           14. The method of claim 12, wherein the forming of the inner  
8           conductive layer comprises electroless plating a conductive material over  
9           the conductive line pattern.

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11          15. The method of claim 12 further comprising prior to vapor  
12          depositing the polymer dielectric material, removing at least some of the  
13          masking material layer.

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15          16. The method of claim 12, wherein the patterning comprises  
16          forming a plurality of conductive line patterns.

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18          17. The method of claim 16 further comprising after forming the  
19          inner conductive layer, planarizing the inner conductive layer relative to  
20          the masking material layer.

1           18. The method of claim 16 further comprising:  
2                 after forming the inner conductive layer, planarizing the inner  
3                 conductive layer relative to the masking material layer; and  
4                 prior to vapor depositing the polymer dielectric material, removing  
5                 at least some of the masking material layer.

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7           19. A method of forming a co-axial line comprising:  
8                 forming a pair of upstanding, spaced-apart conductive terminal  
9                 members over a substrate;  
10                 forming a co-axial inner conductive line component which extends  
11                 between and electrically connects with the terminal members;  
12                 surrounding a substantial portion of the inner conductive line  
13                 component with a dielectric polymer layer; and  
14                 forming a co-axial outer conductive line component over the  
15                 dielectric polymer layer.

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17           20. The method of claim 19 further comprising forming a  
18                 masking material trough which extends between exposed portions of the  
19                 terminal members, at least a portion of the inner conductive line  
20                 component being formed within the trough.

1        21. The method of claim 19, wherein the forming of the co-  
2        axial inner conductive line component comprises:

3              forming a masking material over the substrate;  
4              patterning the masking material to form a conductive line pattern  
5        which exposes at least some of the conductive terminal members; and  
6              electrically connecting exposed portions of the conductive terminal  
7        members through the conductive line pattern.

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9        22. The method of claim 21, wherein the electrically connecting  
10      comprises electroplating conductive material at least within the  
11      conductive line pattern.

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13        23. The method of claim 21, wherein the electrically connecting  
14      comprises electroless plating a conductive material at least within the  
15      conductive line pattern.

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17        24. The method of claim 19, wherein the dielectric polymer  
18      layer comprises Parylene.

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20        25. The method of claim 19, wherein the forming of the co-  
21        axial outer conductive line component comprises chemical vapor  
22        depositing a metal-comprising layer over the dielectric polymer layer.

1        26. The method of claim 19, wherein the forming of the co-  
2        axial outer conductive line component comprises electroless plating the  
3        line component over the dielectric polymer layer.

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5        27. A method of forming a co-axial line comprising:  
6              forming a pair of upstanding, spaced-apart terminal members over  
7        a substrate;  
8              forming photoresist over the terminal members;  
9              forming a line pattern within the photoresist which exposes and  
10        extends between the terminal members;  
11              sputtering a first conductive layer of material over the co-axial  
12        line pattern;  
13              electroplating a second conductive material over the first  
14        conductive layer;  
15              forming a dielectric layer over the second conductive material  
16        surrounding a substantial portion thereof; and  
17              forming an outer conductive sheath of material over the dielectric  
18        layer.

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20        28. The method of claim 27, wherein the sputtering of the first  
21        conductive layer comprises ionized magnetron sputtering of the first  
22        conductive layer.

1           29. The method of claim 27, wherein the forming of the  
2 dielectric layer comprises forming a polymer layer over the second  
3 conductive material.

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5           30. The method of claim 27 further comprising after the  
6 electroplating of the second conductive material:

7                 planarizing the second conductive material relative to the  
8 photoresist; and

9                 prior to the forming of the dielectric layer, removing the  
10 photoresist from around the second conductive material.

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12           31. A method of forming a co-axial line comprising:  
13                 forming a pair of upstanding, spaced-apart terminal members over  
14 a substrate;  
15                 forming photoresist over the terminal members;  
16                 forming a line pattern within the photoresist which exposes and  
17 extends between the terminal members;  
18                 electroless plating a conductive material over the co-axial line  
19 pattern;  
20                 forming a dielectric layer over the conductive material; and  
21                 forming an outer conductive sheath of material over the dielectric  
22 layer.

1           32. The method of claim 31, wherein the forming of the  
2 dielectric layer comprises forming a polymer layer over the electroless-  
3 plated conductive material.

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5           33. The method of claim 31 further comprising after the  
6 electroless plating of the conductive material:

7                 planarizing the electroless-plated conductive material relative to the  
8 photoresist; and

9                 prior to the forming of the dielectric layer, removing the  
10 photoresist from around the electroless-plated conductive material.

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1       34. A method of forming a co-axial line comprising:

2              providing a substrate having an outer surface;

3              forming a pair of upstanding, spaced-apart conductive terminal

4              members over the substrate outer surface;

5              forming a layer of photoresist over the substrate outer surface;

6              forming a conductive line pattern in the photoresist, the

7              conductive line pattern extending at least between and exposing portions

8              of the conductive terminal members;

9              forming a layer of conductive material over the substrate and

10             within the conductive line pattern;

11             removing a sufficient amount of material of the layer of

12             conductive material to electrically isolate the conductive material within

13             the conductive line pattern;

14             removing photoresist from at least around a conductive material

15             portion which extends between the spaced-apart conductive terminal

16             members, the removing of the photoresist leaving the conductive material

17             portion supported above underlying substrate outer surface;

18             vapor depositing a polymer dielectric material comprising Parylene,

19             the depositing of the Parylene completely surrounding the conductive

20             material portion which extends between the spaced-apart conductive

21             terminal members; and

22             vapor depositing a conductive material at least over the Parylene

23             which surrounds the conductive material portion which extends between

24             the spaced-apart conductive terminal members.

1       35. Integrated circuitry comprising:  
2           a semiconductive substrate having an outer surface;  
3           an inner conductive core spaced from and over the outer surface;  
4           a polymer dielectric layer surrounding a substantial portion of the  
5           inner conductive core; and  
6           an outer conductive sheath surrounding a substantial portion of  
7           the polymer dielectric layer.

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9       36. Integrated circuitry comprising:  
10          a semiconductive substrate having an outer surface;  
11          a pair of spaced-apart terminal members disposed over the outer  
12          surface and extending elevationally away therefrom;  
13          an inner conductive core operably connected with and extending  
14          between the spaced-apart terminal members;  
15          a polymer dielectric layer over a substantial portion of the inner  
16          conductive core; and  
17          an outer conductive sheath surrounding a substantial portion of  
18          the polymer dielectric layer.

1           37. Integrated circuitry comprising:

2            a substrate having an outer surface;

3            a pair of upstanding, spaced-apart conductive terminal members

4            disposed over the substrate outer surface;

5            a copper-comprising layer of material operably connected with and

6            extending between the terminal members, the copper-comprising layer

7            having a thickness of between about 100 to 200 nanometers;

8            a conductive layer of material disposed over and operably

9            connected with the copper-comprising layer of material, the conductive

10          layer comprising conductive material selected from the group consisting

11          of copper, gold, nickel, cobalt, and iron;

12          a dielectric layer comprising Parylene disposed over the conductive

13          layer of material, the dielectric layer surrounding conductive layer

14          portions which extend between the terminal members; and

15          an outer conductive sheath of material disposed over the dielectric

16          layer and surrounding dielectric layer portions which extend between the

17          terminal members.

FATIGUE TEST SHEET